2.2.F Atmega-Peripherie/Timer – Ergänzungen und Bilder

2.2.F.1 Prinzipaufbau des Timers 0

Name										Adresse
	Bit	7	6	5	4	3	2	1	0	
TIMSK		OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	SFR 57
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	
	Bit	7	6	5	4	3	2	1	0	
TIFR		OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	–	TOV0	SFR 56
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	
	Bit	7	6	5	4	3	2	1	0	
TCCR0		–	–	–	–	–	CS02	CS01	CS00	SFR 51
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	
	Bit	7	6	5	4	3	2	1	0	
TCNT0		TCNT07	TCNT06	TCNT05	TCNT04	TCNT03	TCNT02	TCNT01	TCNT00	SFR 50
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	

Tabelle 1: Register für Timer 0 (ATmega 8, 16, 32)

Name										Adresse
	Bit	7	6	5	4	3	2	1	0	
TIMSK0		–	–	–	–	–	OCIE0B	OCIE0A	TOIE0	RAM 110
	R/W	R	R	R	R	R	R/W	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	
	Bit	7	6	5	4	3	2	1	0	
TIFR0		–	–	–	–	–	OCF0B	OCF0A	TOV0	SFR 21
	R/W	R	R	R	R	R	R/W	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	
	Bit	7	6	5	4	3	2	1	0	
TCCR0A		COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	SFR 36
	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	
	Bit	7	6	5	4	3	2	1	0	
TCCR0B		FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	SFR 37
	R/W	W	W	R	R	R/W	R/W	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	
	Bit	7	6	5	4	3	2	1	0	
TCNT0		TCNT07	TCNT06	TCNT05	TCNT04	TCNT03	TCNT02	TCNT01	TCNT00	SFR 38
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	
	Bit	7	6	5	4	3	2	1	0	
OCR0A		OCR0A7	OCR0A6	OCR0A5	OCR0A4	OCR0A3	OCR0A2	OCR0A1	OCR0A0	SFR 39
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	
	Bit	7	6	5	4	3	2	1	0	
OCR0B		OCR0B7	OCR0B6	OCR0B5	OCR0B4	OCR0B3	OCR0B2	OCR0B1	OCR0B0	SFR 40
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Init.	0	0	0	0	0	0	0	0	

Tabelle 2: Register für Timer 0 (ATmega164, 324, 644, 1284p)

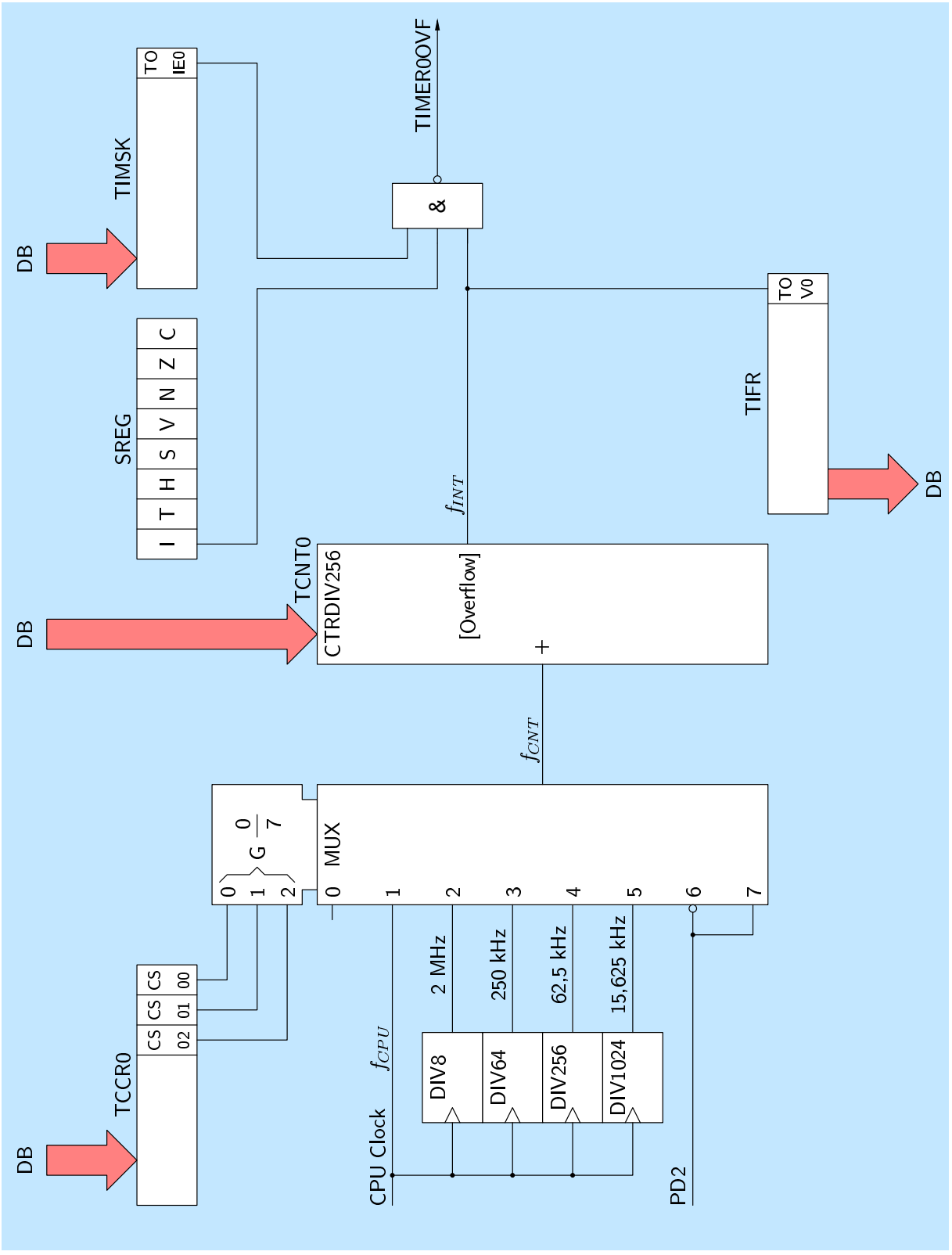

Abbildung 1: Prinzipaufbau des Timers 0